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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/832,884	04/12/2001	Steve M. Danziger	L/M-102-DIV	2718
7590		05/06/2004	EXAMINER	
Ronald R. Snider		PERT, EVAN T		
Snider & Associates		ART UNIT		
P.O. Box 27613		2829		
Washington, DC 20038-7613		PAPER NUMBER		

DATE MAILED: 05/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application N .

09/832,884

Applicant(s)

DANZIGER ET AL.

Examiner

Evan Pert

Art Unit

2829

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 26 February 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1,2 and 5-7 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,2 and 5-7 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 112***

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-2 and 5-7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Applicant may claim a product by process limitations so long as the process limitations are clearly directed to the product [MPEP 2173.05(p)].

In the instant case, applicant's claimed product is ambiguous because of process limitations not clearly directed to the product:

In claim 1, the limitation "which is thermal stress tolerance tested prior to mounting...by a test device" is clearly directed to the process, but not the product. What structure necessarily results from this process limitation? For purposes of examination, this process limitation bears insignificant patentable weight for the product, since a person has no way to structurally discern that something was "stress tolerance tested prior to mounting."

In claim 1, the last six lines are directed to how the earlier recited "solder ball array connections" and "wire bond connections" are "used" and "connected" and "not connected" at various points in time during a *process*. The acts do not give rise to a clearly discernable structure in the finally claimed product; what do the "wire bond connections" and "solder ball array connections" physically look like in the product?

In claim 2, connections "remain pristine" until a certain time, which is a process limitation not clearly directed to the product. If they remain pristine until a time, what do they look like in the product compared prior art connections that are "not pristine" and were never pristine?

In claim 5, "connections" are recited such that they are "not removed from the die." When "connections" are "not removed from the die," dependent claim 5 is not further limiting. When "connections" are "removed," independent claim 1 is confusing because it implicitly recites a device "having" the "connections" that were "removed."

For purposes of examination, the "solder ball connections" and "wire bond connections" of the claimed product are any discernable electrical contact structures that *are* or *were* "solder ball connections" or "wire bond connections," respectively.

***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-2 and 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Galloway (U.S. 5,886,414) in view of a flip-chip package reference to Shaukatullah et al. (IEEE 1995) taken with a flip-chip package reference to Sherif et al. (US 5,623,394).

**What Galloway Teaches:**

**Claim 1**

Regarding claim 1, Galloway discloses an end use device (Fig. 9, 88 or 90) having a known good die (col. 5, line 16), the KGD having solder bump array (24 of Fig. 8A with col. 3, lines 31-32) and wire bond connections (92 of Fig. 8A); the KGD having solder bump array connections on a planar KGD surface (e.g. bumps 24 are "on" and "over" the upper planar surface of the KGD 14); the KGD having an array of wire bond connections (i.e. the array of wire bond connections 92 that correspond to the bump array 24) on the planar KGD surface; the KGD having electrical connections between of the solder bump array connections and the wire bond connections [col. 3]; wherein the KGD is a KGD which is thermal stress tolerance tested prior to mounting the KGD on the end use device by a test device connected to the KGD by the wire bond connections or in the alternative by the solder ball connections (i.e. Step 84 of Fig. 9); wherein when either the wire bond connections are used or the solder ball connections are used for a known good die test, the other connections are connected to the end use device [col. 5, lines 19-21]; and the connections used for the known good die test are not connected to the end use device or any other device, when the KGD is connected to the end use device [cols. 4-5].

**What Galloway Teaches (continued):**

**Claim 2**

Regarding claim 2, Galloway discloses that the end use device in accordance with his invention includes a teaching that the wire bond connections are damaged for KGD testing, while the bump connections 24 are not affected by the known good die (KGD) test and remain pristine (i.e. undamaged) [cols. 4-5].

**Claim 5**

Galloway discloses that the wire bond connections are "optionally removed" at Step 86 of Fig. 9.

**Claim 6**

Galloway discloses that the connections to the test device are metallurgical connections (i.e. the electrical connections involve metal and bonding of metal).

**What Galloway Does Not Teach:**

**Claims 1, 2, 5 and 6**

Galloway is silent about "solder *ball* array," but mentions the notoriously well known application of metal bumps 24 for a "flip-chip" [col. 3, line 30].

**Claim 7**

Galloway is silent that metal bumps 24 (for a "flip-chip") are a "solder ball array" of "controlled collapse chip connections."

**What the Secondary References Teach:**

Both Shaukatullah et al. and Sherif et al. disclose "controlled collapse chip connections," which are notoriously well known for joining of "flip-chips" using small "solder balls" that "are capable of providing a very large number of input and output connections" [p. 865, Shaukatullah].

Sherif et al. explain that "solder connections" in general for a "flip-chip" are accomplished by "solder connections, such as, for example, C4 (Control Collapse Chip Connection), solder balls, solder column connection, or ball grid arrays." Thus, Sherif et al., lists C4 as a choice for making flip-chip connections such as for the gold bumps 24 disclosed by Galloway.

**Obvious to Modify Bumps 24 in Galloway to Include C4 Solder Balls:**

It would have been obvious to one of ordinary skill in the art at the time of the claimed invention to modify the metal bumps 24 of Galloway to include "solder balls" in a "controlled collapse chip connection (C4)" process. One of ordinary skill would be motivated, for example, by the teaching of Shaukatullah et al. that "C4 type of flip-chips are capable of providing a very large number of input and output connections" [p. 865, upper right column].

***Response to Arguments***

3. Applicant's arguments with respect to claims 1-2 and 5-7 have been considered but are moot in view of the new grounds of rejection.

**Conclusion**

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Evan Pert whose telephone number is 703-306-5689. The examiner can normally be reached on M-F (7:30AM-3:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 703-308-1233. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ETP  
April 27, 2004

  
**EVAN PERT**  
**PRIMARY EXAMINER**